International Journal of Applied Engineering and Technology ISSN: 2277-212X (Online)
Online International Journal Available at http://www.cibtech.org/jet.htm
2020 Vol. 9, pp.197-201/Mukesh et al.
***Research Article** (Open Access)*

A DESIGN OF LOW POWER AND HIGH SPEED CONFIGURABLE ADDER FOR APPROXIMATE COMPUTING

S. Mukesh Ram, S. Saravanan, M. Srinath, B. Venkatesh and *A. Surya
Department of Electronics and Communication Engineering,
Anjalai Ammal Mahalingam Engineering College, Tiruvarur

ABSTRACT
Approximate computing is an efficient approach for error-tolerant applications because it can trade off accuracy for power. Addition is a key fundamental function for these applications. In this paper, we proposed a low-power yet high speed accuracy-configurable adder that also maintains a small design area. The proposed adder is based on the conventional carry look-ahead adder, and its configurability of accuracy is realized by masking the carry propagation at runtime. Compared with the Existing conventional carry look-ahead adder Design, the proposed 32-bit adder reduced Area, power consumption and critical path delay. This Proposed Design is implemented by Verilog HDL and Simulated using Modelsim 6.4c. The Synthesis Part is done by Xilinx.

***Keyword*:** *Approximate Computing, Accuracy-Configurable Adder, High-Speed Adder, Low-Power Adder*

INTRODUCTION
The power consumption reduction and speed improvement are the key goals in the design of digital processing units, especially the portable systems. Normally, an increase in the speed is achieved at the cost of more power consumption for exact processing units. One of the approaches to improve both the power and speed is to sacrifice the computation exactness. This approach, which is approximate computing, may be used for the applications where some errors may be tolerated. Approximate computing is a computation technique which returns a possibly inaccurate result rather than a guaranteed accurate result, and can be used for applications where an approximate result is sufficient for its purpose. Applications that have recently emerged such as image recognition and synthesis, digital signal processing, which is computationally demanding, and wearable devices, which require battery power have created challenges relative to power consumption. Addition is a fundamental arithmetic function for these applications. Most of these applications have an inherent tolerance for insignificant inaccuracies. By exploiting the inherent tolerance feature, approximate computing can be adopted for a tradeoff between accuracy and power. At present, this tradeoff plays a significant role in such application domains.

PROPOSED SYSTEM
A CLA consists of three parts: (1) half adders for carry generation (G) and propagation (P) signals preparation, (2) carry look-ahead units for carry generation, and (3) simple adder for sum generation. We focus on the half adders for G and P signals preparation in part 1. Consider an n-bit CLA;where I is denoted the bit position from the least significant bit. Note that owing to reuse of the circuit of Ai XOR Bi for Si generation, here Pi is defined as Ai XOR Bi instead of Ai OR Bi. Because C0 is equal to G0, if G0 is 0, C0 will be 0. From (2), we find that C1 is equal to G1 when C0 is 0. In other words, if G0 and G1 are equal to 0, C0 and C1 will be 0. By expanding the above to i, Ci will be 0 when G0, G1…, Gi are all 0. This means that the carry propagation from C0 to Ci is masked. From (3), we can obtain that Si is equal to Pi when Ci-1 is 0.

$$Pi = Ai \oplus Bi,\ Gi = Ai \cdot Bi, \quad (1)$$
$$Ci = Gi + Pi \cdot Ci\text{-}1, \quad (2)$$
$$Si = Pi \oplus Ci\text{-}1. \quad (3)$$

We find that C1 is equal to G1 when C0 is 0. In other words, if G0 and G1 are equal to 0, C0 and C1 will be 0. By expanding the above to i , Ci will be 0 when G0, G1, … , Gi are all 0. This means that the carry propagation from C0 to Ci is masked. We can obtain that Si is equal to Pi when Ci-1 is 0.

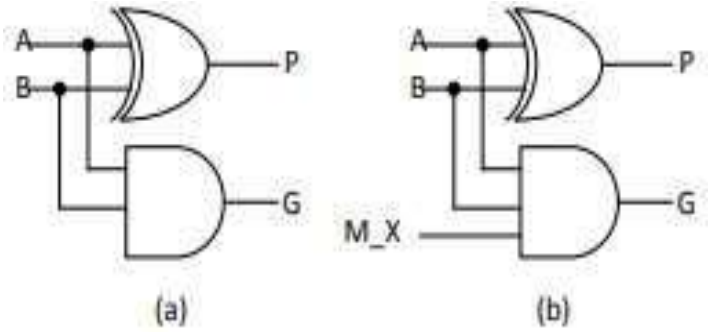

Figure1: (a) An accurate half adder, and (b) a half adder with a select signal.

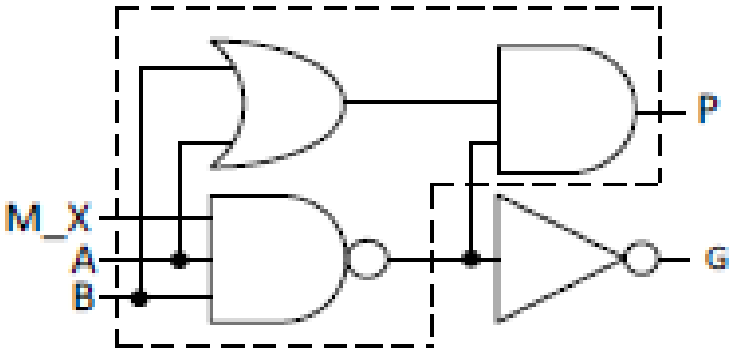

Figure2: A carry-maskable half adder.

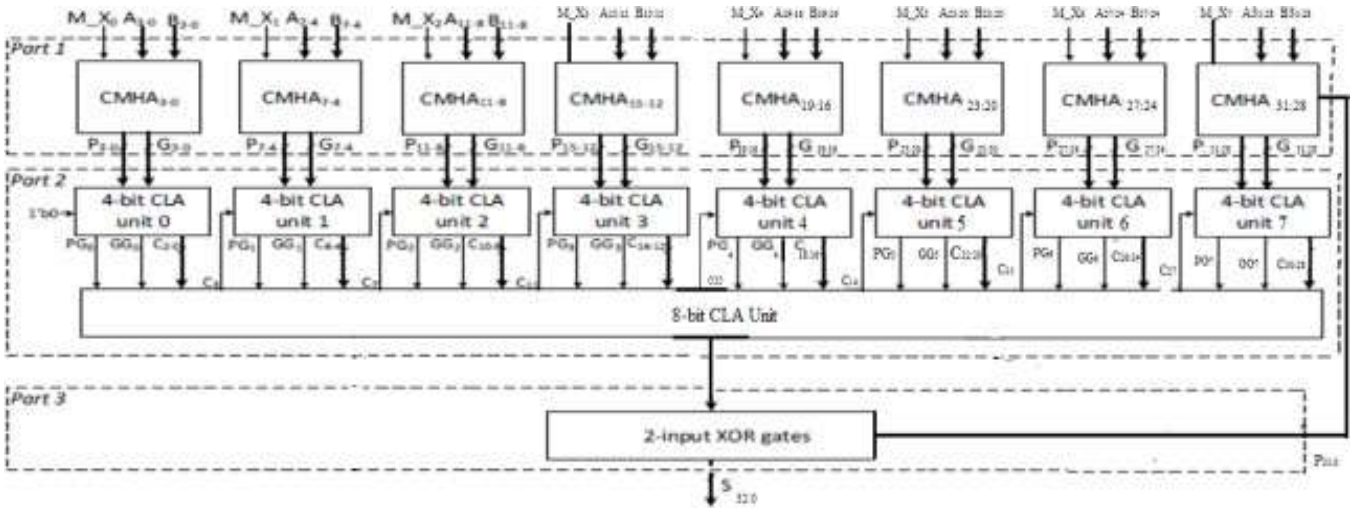

Figure 3: Structure of the proposed 16-bit adder.

From the point of view of approximate figuring, if G is controllable and can be controlled to be 0, the carry propagation will be covered and S (=P) can be considered as an approximate whole. As it were, we can get

the selectivity of S between the exact and approximate entirety on the off chance that we can control G to be An AND B or 0. Clearly, we can accomplish selectivity by including a select flag. Figure 1(a) is an ordinary half adder and Fig. 1(b) is a half adder to which the select flag has been included. Contrasted and the traditional half adder, we include a flag named "M_X" as the select flag and utilize a 3-info AND entryway to supplant the 2- input one. At the point when M_X = 1, the capacity of G is equivalent to that of a customary half adder; when M_X = 0, G is equivalent to 0

EXPERIMENTAL RESULTS

DEVICE UTILIZATION

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	99	66,560	1%	
Logic Distribution				
Number of occupied Slices	57	33,280	1%	
Number of Slices containing only related logic	57	57	100%	
Number of Slices containing unrelated logic	0	57	0%	
Total Number of 4 input LUTs	99	66,560	1%	
Number of bonded IOBs	98	784	12%	
Total equivalent gate count for design	594			
Additional JTAG gate count for IOBs	4,704			

Figure 4: Shows the device utilization of 32 bit existing adder

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	64	66,560	1%	
Logic Distribution				
Number of occupied Slices	48	33,280	1%	
Number of Slices containing only related logic	48	48	100%	
Number of Slices containing unrelated logic	0	48	0%	
Total Number of 4 input LUTs	64	66,560	1%	
Number of bonded IOBs	100	784	12%	
IOB Flip Flops	33			
Number of GCLKs	1	8	12%	
Total equivalent gate count for design	840			
Additional JTAG gate count for IOBs	4,800			

Figure 5: Shows the device utilization of 32 bit proposed adder

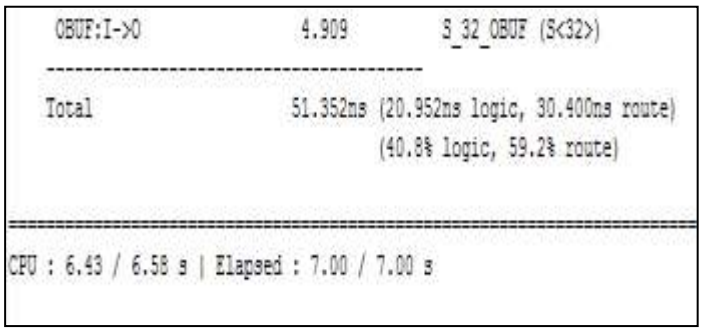

Figure 6: Shows the delay of 32 bit existing adder

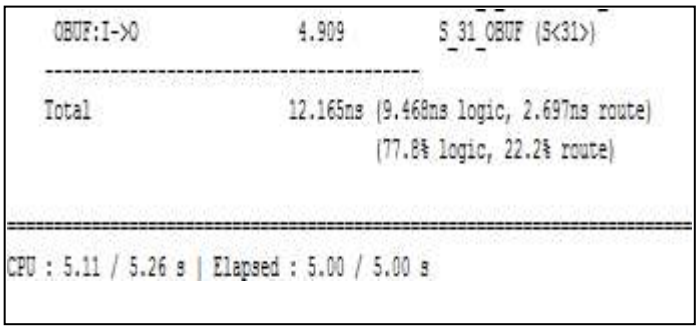

Figure 7: Shows the device delay of 32 bit proposed adder

CONCLUSION

In this paper, an accuracy-configurable adder without suffering the cost of the increase in power for configurability was proposed. The proposed adder is based on the conventional CLA, and its configurability of accuracy is realized by masking the carry propagation at runtime. The experimental results demonstrate that the proposed adder delivers significant power savings and speedup with a small area overhead than those of the conventional CLA. Furthermore, compared with previously studied configurable adders, the experimental results demonstrate that the proposed adder achieves the original purpose of delivering an unbiased optimized result between power and delay without sacrificing accuracy. It was also found that the quality requirements of the evaluated application were not compromised.

REFERENCES

Liang J, J Han and F. Lombardi (2013). *New metrics for the reliability of approximate and probabilistic adders, IEEE Transactions on Computers*, **62**(9)1760-1771.

Venkatesan R, A Agarwal, K Roy and A Raghunathan (2011). MACACO: modeling and analysis of circuits for approximate computing, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 667-673.

Gupta V, D Mohapatra, A Raghunathan and K Roy (2013). Low-Power digital signal processing using approximate adders, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, **32** (1)124-137.

Ye R, T Wang, F Yuan, R Kumar and Q Xu (2013). *On Reconfiguration Oriented Approximate Adder Design and Its Application, IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 48-54.

Venkataramani S, V K Chippa, S T Chakra Dhār, K Roy and A Raghunathan (2013). Quality programmable vector processors for approximate computing, 46th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO) 1-12.