

OPTIMIZED EXTENDED TRUE-SINGLE-PHASE-CLOCK (E-TSPC) FREQUENCY DIVIDER USING 0.05 μ M CMOS TECHNOLOGY

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ABSTRACT

In this paper, the optimized extended true-single-phase-clock (E-TSPC) frequency dividers using 0.05 μ m CMOS technology is presented. The ratio MOSFETs are designed in such a way that the operating frequencies of E-TSPC divide-by-2 and E-TSPC 2/3 Prescaler have been considerably increased and the power consumption has been decreased comparing to the past. Optimized extended true-single-phase-clock (E-TSPC) frequency divider is operated using supply voltage of 0.9V and frequency of more than 1250GHz. The divider was simulated with square frequency up to 1250GHz and with 50% duty-cycle and its power consumption in the highest frequency is 5.49uW which is dramatically less than previously reported amounts.

Keywords: *Extended TSPC, Frequency Divider, Frequency Synthesizer, Low Power Consumption*

INTRODUCTION

Integrated circuits with radio frequency and low power consumption have increasingly attracted the attentions. Battery life duration is of crucial importance for the mobile and wireless communications that work with low power consumption. Low power consumption is of great importance in this regard and it also reduces the temperature and leads to stability. On the other hand the need for high speed and two-way communication system due to ever developing world can be a necessity for personal affairs and trades. However the new wireless applications (e.g. the above high quality image) need band width crucially. To solve this problem we need to allocate new bands frequency and GHz spectrum rang (Krishna *et al.*, 2010). We need a high-frequency signal generator in the transmitter and receiver whose signal can be square or sinusoidal depending on the type of modulation. Signal generator in transmitters and receivers is called, local oscillator. The frequency and phase of signal in transmitter local oscillator have to be the same as the frequency and phase of the receiver local oscillator according to the modulation. Local oscillator in the modern transmitters and receivers is a frequency synthesizer. Frequency synthesizer produces precise and stable signals according to reference frequency. Reference frequency is generated by crystal oscillator with high stability but its frequency is low for transmitter and receiver uses (Arifin *et al.*, 2012). Phase locked loop (PLL) is often used in the frequency synthesis as local oscillator for up-converting in transmitters and for down-converting in receivers. A PLL is composed of 4 main parts namely: phase detector, loop filter (LPF), voltage-controlled oscillator (VCO), and frequency divider (including a prescaler) (Mujiono, 2003). Frequency divider is one of the building blocks of a PLL frequency synthesizer that converts high frequency of oscillator output to lower frequency that can be compared with reference frequency. The maximum operating frequency of a frequency divider is dependent on the style of architecture, feeding voltage, and output load.

Current mode logic (CML) static divider (Lee and Liu, 2007), miller divider (Lee and Razavi, 2004), and injection-locked frequency divider (ILFD) (Mayr *et al.*, 2007; Lin and Liu, 2009) are frequency dividers that are conventionally used in the frequency synthesizer circuits and other applications. CML divider has a high locking range but low operating frequency and high power consumption. ILFDs have limited locking range and high operating frequency. Miller divider, such as ILFDs has limited locking range and high frequency. Power consumption is low in ILFDs and miller, and high in CML. CML latches have one problem which is high load capacitance.

True-single-phase-clock (TSPC) dividers are known as dividers with low power consumption as compared to CML but their operating frequency is less than CML. The logic gates of TSPC have replaced

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CML even in high frequencies thanks to rapid development of CMOS technology and improvement the speed of devices. A divider is designed based on counter just with dynamic logic FFs (flip-flap) like TSPC. Each TSPC flip flap contains 3 stories and each story contains 3 transistors. Such design can be improved more using extended true-single-phase-clock (E-TSPC) FFs. In order to improve the speed and operating power consumption E-TSPC designs canceled the transistor stacked structure so that all the transistors are free from the body effect. Each E-TSPC flip-flap is composed of 6 transistors which are appropriate to operate in high frequency with low power consumption (Suganthi *et al.*, 2012). The present paper aims to investigate the optimization of length to width ratio in flip-flap E-STPC transistors leading to considerable increase of operating frequency and decrease of power consumption.

In this paper an extended true-single-phase-clock (E-TSPC) divide-by-2 high-speed and low power consumption E-TSPC frequency dividers with $0.05\mu\text{m}$ CMOS process is presented. The proposed structure operates up to 1500GHz and consumes less than $7.54\mu\text{W}$ from 0.9V supply voltage. Optimized E-TSPC flip-flop is used in prescaler 2/3 and simulation results indicate a significant increase in frequency and a sharp reduction in power consumption as compared to the previous reports. Section 2 discusses design and analysis. Section3 discusses optimized E-TSPC divide-by-2 and prescaler2/3. Section 4 shows simulation and measurement results. Finally, gives the conclusion.

Analysis of Extended-TSPC (E-TSPC)

E-TSPC divide-by-2 is made of one E-TSPC flip-flap. The divider has three stories and each story has two enhancement-modes MOSFET and the transistors are free from the body effect. They are appropriate to operate in high frequency and low voltage power supply (Suganthi *et al.*, 2012). The ratio of MOSFET transistors are of great importance in such dividers. Figure (1), displays the E-TSPC divide-by-2 using E-TSPC flip-flap.

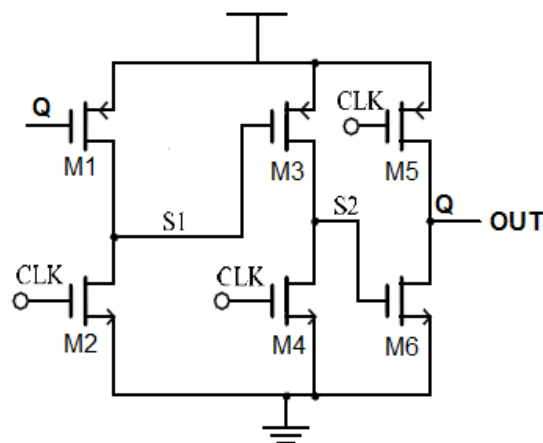


Figure 1: E-TSPC divide-by-2

The circuit operates in pre-charge and evaluation modes. In the pre-charge mode and before the operation of falling edge of the clock, the clock is high and Q is low and the node S2 is pre-charged lowly and when the ratio of M1 is greater than M2 then S1 has high value. M2 and M4 are in the cut area in the falling edge of clock. M1 is still connected so the output Q gets charged more rapidly than node S2 and M2 remains in the cut area. So in the pre-charge mode, node S2 has the low and the node Q has the high value. In the evaluation mode are connected to the raising edge of the clock, M3 and M4 are also connected and operate in the triode region and the node S1 gets discharged rapidly and M3 is on. To have appropriate voltage operation on node S2 and the ratio of M4 has to be larger than M3. So M6 remains in the cut area and Q keeps the high value. M6 needs to be greater than M5 and M1 needs to be greater than M2 (Du *et al.*, 2006). This divider needs only one clock to prevent clock skew. The load capacitive of E-TSPC divider is determined using equation (1). Switching power depends on load capacitance as described by equation (2).

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$$C_L = C_{dbM6} + C_{gdM6} + C_{dbM5} + C_{gdM5} + C_{gM1} \quad (1)$$

$$PSW = F_{CLK} \cdot C_L \cdot V_{dd}^2 \quad (2)$$

Where F_{CLK} is the clock frequency and C_L is the load capacitive and V_{dd} is the power supply voltage. In specific time during this period a direct route is created between the supply and ground called short-circuit power. The power of short-circuit on the MOSFETs ratio and input duty cycle. Due to smaller capacitive load of E-TSPC flip-flops, they consume less switching power but, comparing to TSPC flip-flops, they have more short-circuit power (Yu *et al.*, 2006). Consumption in E-TSPC dividers depends on signal dc level and its range.

MATERIALS AND METHODS

E-TSPC divider has been optimized for very low power consumption and very high operating frequency. E-TSPC divide-by-2 is the basis of modern high frequency and low power consumption prescaler design. Prescaler is one of the most power consuming and challenging parts of the modern synthesizer circuits because it works in the highest frequency and has the highest power consumption. Minimizing the width of transistors and reducing the supply voltage of E-TSPC divider have important roles in lowering power consumption. This type of dividers, use the capacitive load in the nodes for maintaining the mode. The capacitances get charged and discharged through creating a Chanel between the drain and supply so the constant time of charging and discharging rout have to be decreased in higher frequencies to prevent reducing the charge of the voltage. To reduce the time constant we should increase the width of the transistor. So to avoid reducing the voltage at nodes, wider transistors and higher supply voltage are required. Input frequency and band width play crucial roles in optimization of E-TSPC divider that means in higher frequencies we need transistors with wider band and the power consumption increases because when transistor width increases, bigger short circuit current would be created due to direct route from supply to ground. Table 1 shows the width of transistors in different frequencies with the lowest power consumption. The length of all the transistors in the simulation is 0.05um. It is obvious that wider transistors are required in higher operating frequency.

Table 1: The width of Transistors in different frequencies with the lowest power consumption

Frequency (GHz)	The width of Transistors (μm)					
	M1	M2	M3	M4	M5	M6
20	0.2	0.1	0.1	0.2	0.1	0.1
800	0.2	0.1	0.2	0.3	0.2	0.2
1000	0.2	0.1	0.2	0.3	0.2	0.2
1250	0.3	0.2	0.3	0.4	0.2	0.3

Figure (2) shows the circuit of E-TSPC 2/3 prescaler including two E-TSPC flip-flops (Du *et al.*, 2006). The control logic signal MC changes the operation between divide-by-2 and divide-by-3 modes. If MC = '1', the 2/3 prescaler operates in the divide-by-3 mode where the two DFFs actively participate in the operation.

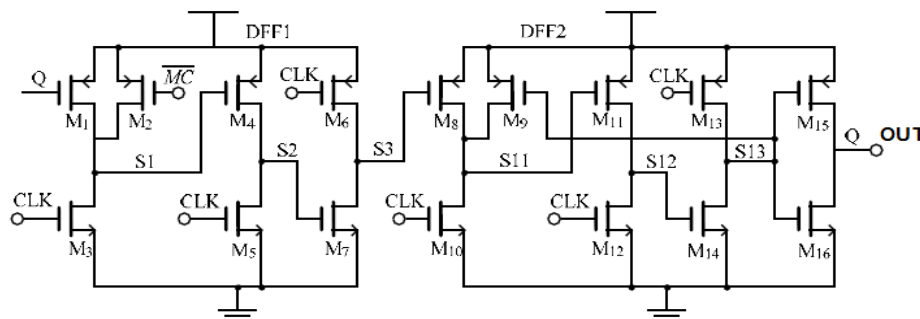


Figure 2: E-TSPC 2/3 prescaler

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During divide-by-2 MC= '0' and PMOS transistor M2 is on, M3 is on for the half of the clock period and at this time there is a route between supply and ground and as a result high short-circuit power. Short-circuit power is available while the clock is high. Short-circuit current gets higher at the first stage transistor M1 is on. In the divide-by-2 mode the nodes S1 and S2 from DFF are '1' and '0' respectively. The transistors M4 and M7 are off and there is inconsiderable short-circuit power in the first and second stages of DFF1 at raise time and fall time. In divide-by-2 mode S1, S2, and S3 nodes are '1', '0', and '1' respectively and remain constant and there is a switching power saving in this mode. So it can't be argued that S1 is always '1' and its amount depends on the sizing of M1, M2, and M3. The power of switching exists thanks to continuous charging and discharging in the first stage of DFF1. If MC='1' then M2 is off and the circuit operates as divide-by-3. The deficiency of this prescaler is that in divide-by-2 mode, DFF1 has the short-circuit and the switching power in the first stage. Power consumption and the frequency of 2/3 prescaler can be improved with optimization of the ratio of transistors. Applying logic gates in the forms of wired-AND, wired-OR, and inverter using the methods combined with flip-flap, we can decrease the number of transistors and power consumption and enhance the operating frequency.

RESULTS AND DISCUSSION

Software hspice is a powerful tool for circuits simulation in high frequency and has the ability to draw the different node waves of the circuit. It can also be used to calculate the power consumption of the circuit. Optimized E-TSPC divider circuit is simulated by this software and the power consumption is calculated in different frequencies. The results indicate that through the optimization of E-TSPC Divider transistor ratio in regarded frequencies the power consumption reduces considerably. With increasing the operating frequency we should increase the width of the transistor channel, this frequency increasing leads to increasing the switching power and increasing of the width leads to increasing the short-circuit current and then short-circuit power. So with increasing the frequency the power consumption considerably increases. Increasing the width of M3 and M4 has no effect on power consumption in this simulation but the increasing of other transistors has a direct effect on power consumption.

Table 2: The Power Consumption of the Optimized E-TSPC divide-by-2 in different frequencies and supply voltage to the square wave with peak voltage equal to dc voltage

Input Frequency (MHz)	20	100	400	800	1000	1250
Square Wave						
Supply Voltage (V)	0.7	0.7	0.7	0.8	0.8	0.9
Average Power (mW)	0.677	0.6774	0.6774	1.3584	2.3477	5.59

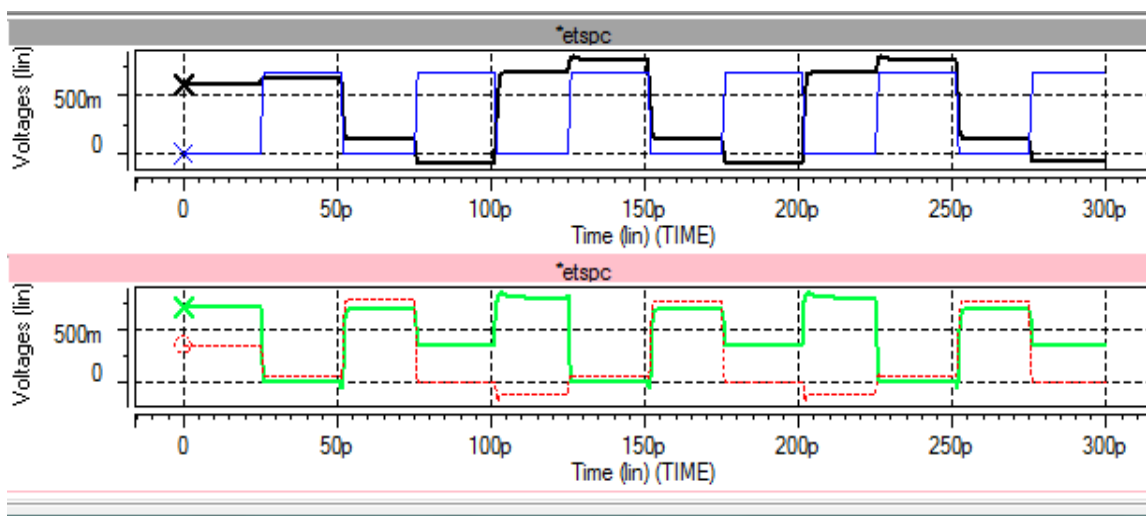


Figure 3: The voltage wave of different parts of the E-TSPC divide-by-2 circuit in 20GHz

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Table 2 shows the power consumption of the optimized E-TSPC divide-by-2 in different frequencies and supply voltage to the square wave with peak voltage equal to dc voltage. The results show that with increasing the input frequency power consumption increases and higher supply voltage is required.

Figure (3) shows the voltage wave of different parts of the optimized E-TSPC divide-by-2 in 20GHz frequency. The blue wave form is input signal, the black one is out node, the green one is S1 node, and the red one is the S2 node. The power consumption in this frequency with supply voltage of 0.7V is 677.403nW which is very low. This circuit is simulated by hspice software in the technology of 0.05um CMOS.

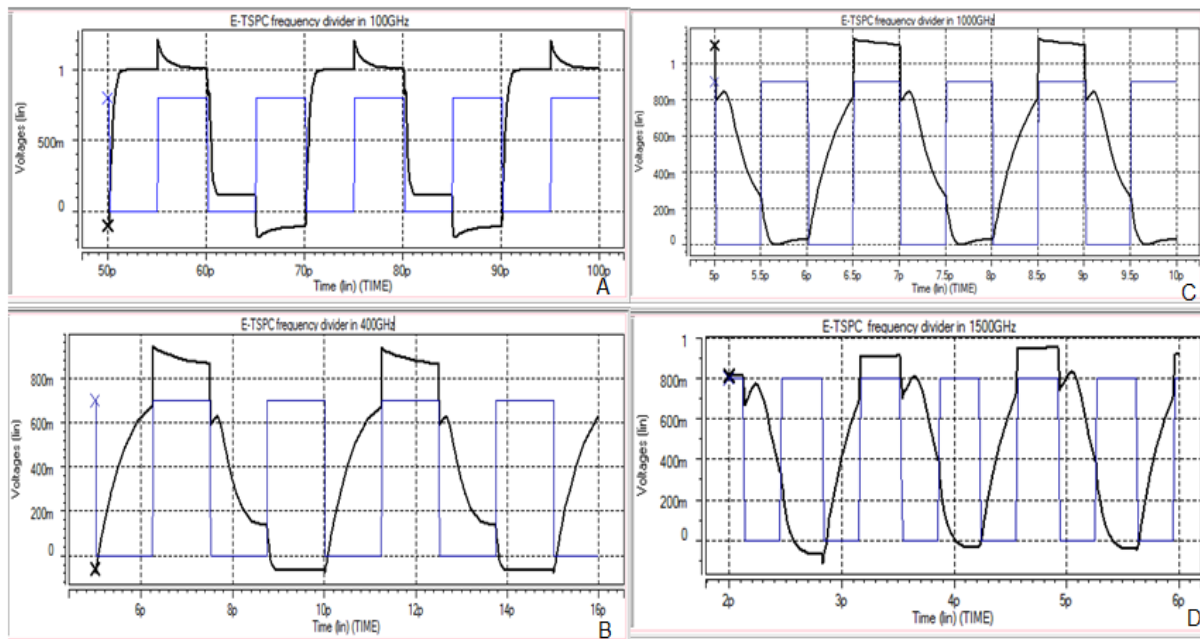


Figure 4: The input and output wave form in, A- 100GHz. B- 400GHz. C- 800GHz. D- 1250 GH.

Figure (4) shows the input and output wave form in 100GHz, 400GHz, 800GHz and 1500GHz frequencies. We need wider width of transistors with the increasing of the frequency to have enough voltage in the circuit nodes.

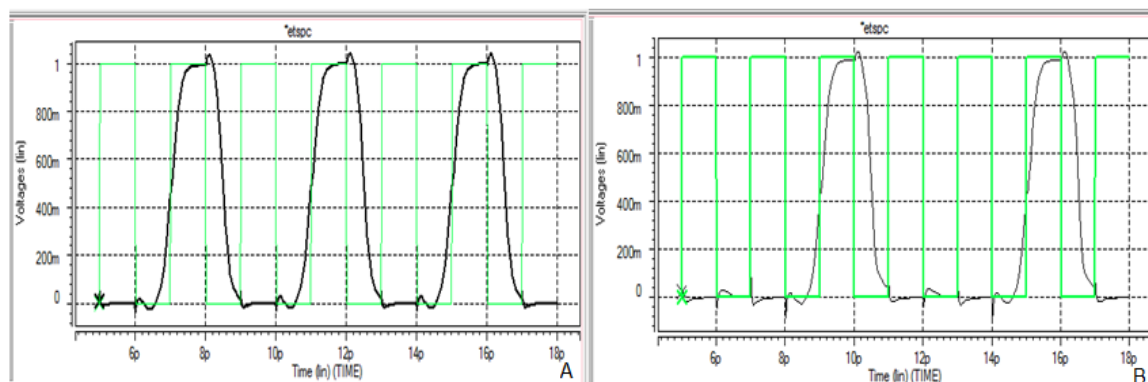


Figure 5: The output waves of 2/3 prescaler in 500GHz to input square wave, A - divide-by-2 mode. B - divide-by-3 mode.

Figure (5) shows the output waves of 2/3 prescaler in 500GHz to input square wave. Comparing to previously reported results the operating frequency and power consumption have been optimized.

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Table 3: The power consumption in E-TSPC divide-by-2, prescaler in divide-by-2 mode, and prescaler in divide-by-3 mode

Divider	E-TSPC Divide-by-2	Prescaler divide- by-2 mode	divide- by-3 mode
Average Power(mW)	0.7574	11.2651	11.2651

Table 3 shows the power consumption in E-TSPC divide-by-2, prescaler in divide-by-2 mode, and prescaler in divide-by-3 mode. As indicated the power consumption in prescaler in divide-by-2 mode is higher than E-TSPC divide-by-2 because in this mode the nodes S1, S2 and S3 remain at logic '1', '0' and '1' respectively although FF1 switch is not active but receive switching and short-circuit power in the first stage. Simulation results indicate that comparing to previously reported circuits, operating frequency has considerably increased and the power consumption decreased.

Using circuits in this technology we will be able to design prescalers, with high frequency and low power consumption.

Conclusion

Optimized extended true-single-phase-clock (E-TSPC) frequency divider with 0.05 μ m CMOS technology have been successfully designed and simulated. Proposed structure operates up to 1250GHz and therefore a 1250GHz square input voltage applies to produce simulation results. Considered E-TSPC frequency dividers have a 50% duty-cycle square output voltage and consumes less than 5.59 μ W power from a 0.9V supply voltage. Simulation results show improvement in speed, area occupation and power consumption as compared to conventional E-TSPC divider. This structure can use in fast-speed, low-noise, low power and small area occupation frequency synthesizer.

REFERENCES

- Arifin MABT, Mamun M, Bhuiyan MAS and Husain H (2012).** Design of a low power and wide band true single-phase clock frequency divider. *Australian Journal of Basic and Applied Sciences* **6** 73-79.
- Bazzazi A and Nabavi A (2009).** Design of a low-power 10GHz frequency divider using extended true single phase clock (E-TSPC) logic. *International Conference on Emerging Trends in Electronic and Photonic Devices & Systems, Varanasi, India* 173-176.
- Deng Z and Niknejad AM (2010).** The speed-power trade-off in the design of CMOS true-single-phase-clock dividers. *IEEE Journal of Solid-state Circuits* **45**(11) 2457-2465.
- Du, Q, Zhuang J and Kwasniewski T (2006).** A low phase noise DLL clock generator with a programmable dynamic frequency divider. *Canadian Conference on Electrical and Computer Engineering (CCECE) Ottawa Canada* 701-704.
- Joshi H and Ranjan SM (2012).** A 1.8 GHz - 2.4 GHz fully programmable frequency divider and a dual-modulus prescaler for high speed frequency operation in PLL system using 250 nm CMOS technology. *International Journal of Engineering Research and Applications* **2**(4) 1510-1517.
- Krishna MV, Do MA, Yeo KS, Boon CC and Lim WM (2010).** Design and analysis of ultra low power true single phase clock CMOS 2/3 Prescaler. *IEEE Transactions on Circuits and Systems* **57**(1) 72-82.
- Lee C and Liu SI (2007).** A 58-to-60.4 GHz Frequency Synthesizer in 90 nm CMOS. *In IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers* 196-197.
- Lee J and Razavi B (2004).** A 40-GHz Frequency Divider in 0.18- μ m CMOS Technology. *IEEE Journal of Solid-State Circuits* **39**(4) 594-601.
- Lin BY and Liu SI (2009).** A 132.7-to-143.5 GHz Injection-locked Frequency Divider in 65 nm CMOS. *Symposium on VLSI Circuits Digest of Technical Papers* 230-231.
- Mayr P, Weyers C and Langmann U (2007).** A 90 GHz 65 nm CMOS Injection-locked Frequency Divider. *In IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers* 198-199.
- Meer, MIY, Gupta AK and Paily RP (2011).** Fractional-n frequency synthesizer design for RF applications. *International Journal of Engineering Science and Technology* **3**(11) 7891-7898.

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Mujiono and T(2003). Design of high frequency CMOS fractional-n frequency divider. *Journal of Electrical and Electronics Engineering* **1**(1) 12-16.

Rana RS (2005). Dual-modulus 127/128 FOM enhanced prescaler design in 0.35 um CMOS technology. *IEEE Journal of Solid-State Circuits* **40**(8) 1662–1670.

Soares JN, Jr and Van Noije WAM (1998). A 1.6-GHz dual modulus prescaler using the extended true-single-phase-clock CMOS circuit technique (E-TSPC). *IEEE Journal of Solid State Circuits* **34**(1) 97–101.

Suganthi J, Kumaresan N and Anbarasi K (2012). Design of power efficient divide by 2/3 counter using E-TSPC based flip flops. *International Journal of Innovative Technology and Exploring Engineering* **1**(2) 158-161.

Yu XP, Do MA, Lim WM, Yeo KS and Ma JG (2006). Design and optimization of the extended true-single-phase-clock based prescaler. *IEEE Transactions on Microwave Theory and Techniques* **54**(11) 3828-3835.